

0503-A30136-USf/Yianhow/Eric

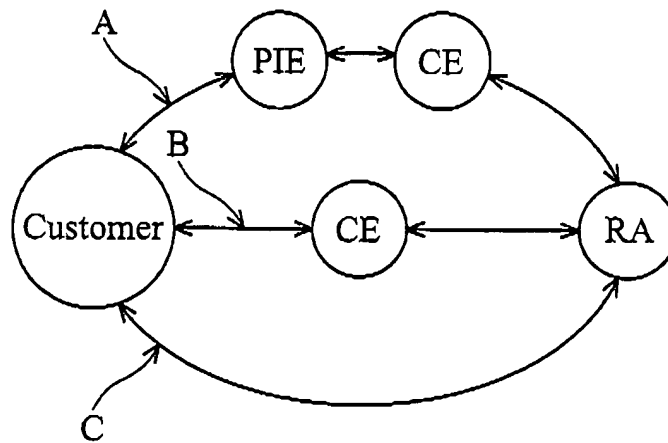


FIG. 1 (RELATED ART)

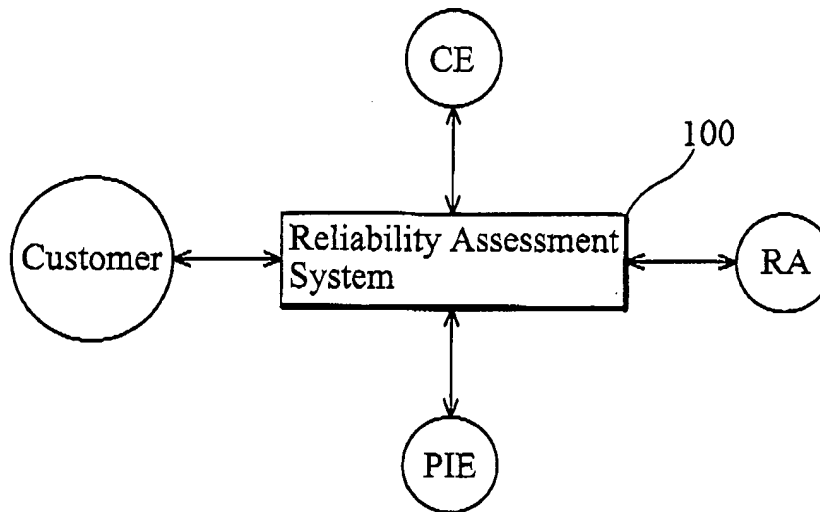


FIG. 2

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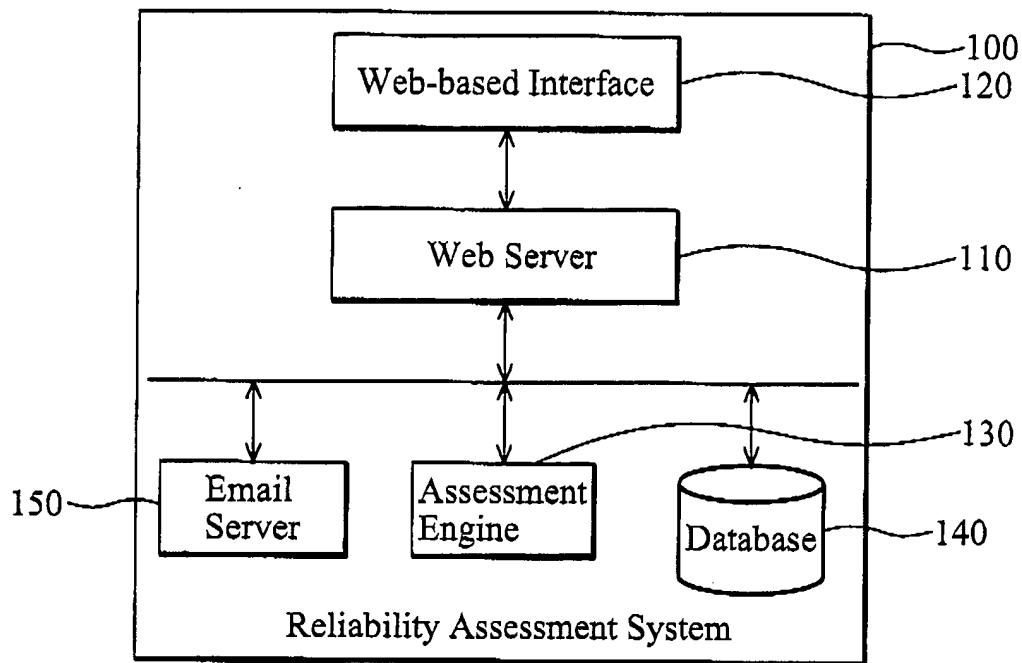


FIG. 3

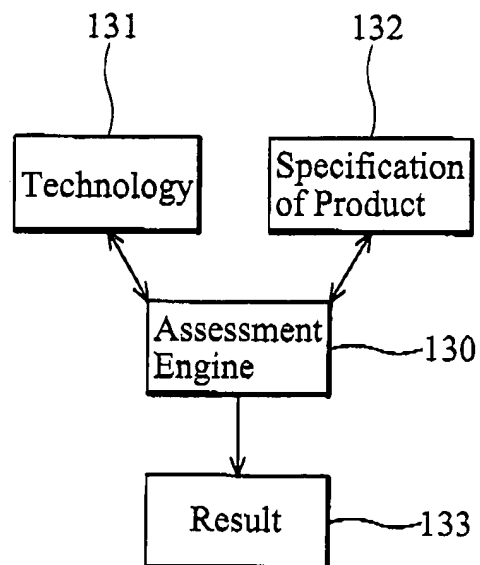


FIG. 4

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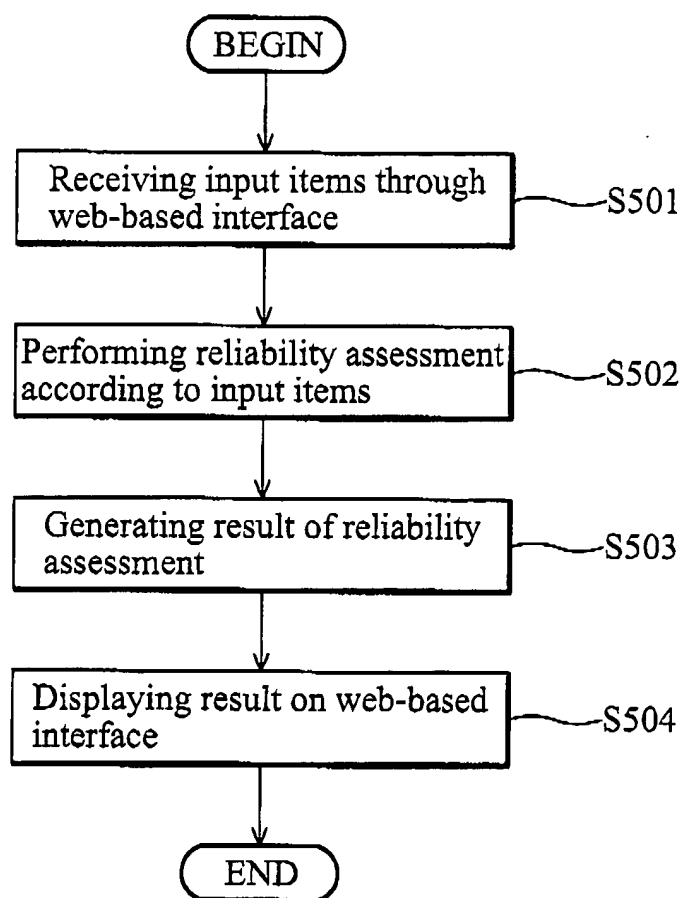


FIG. 5

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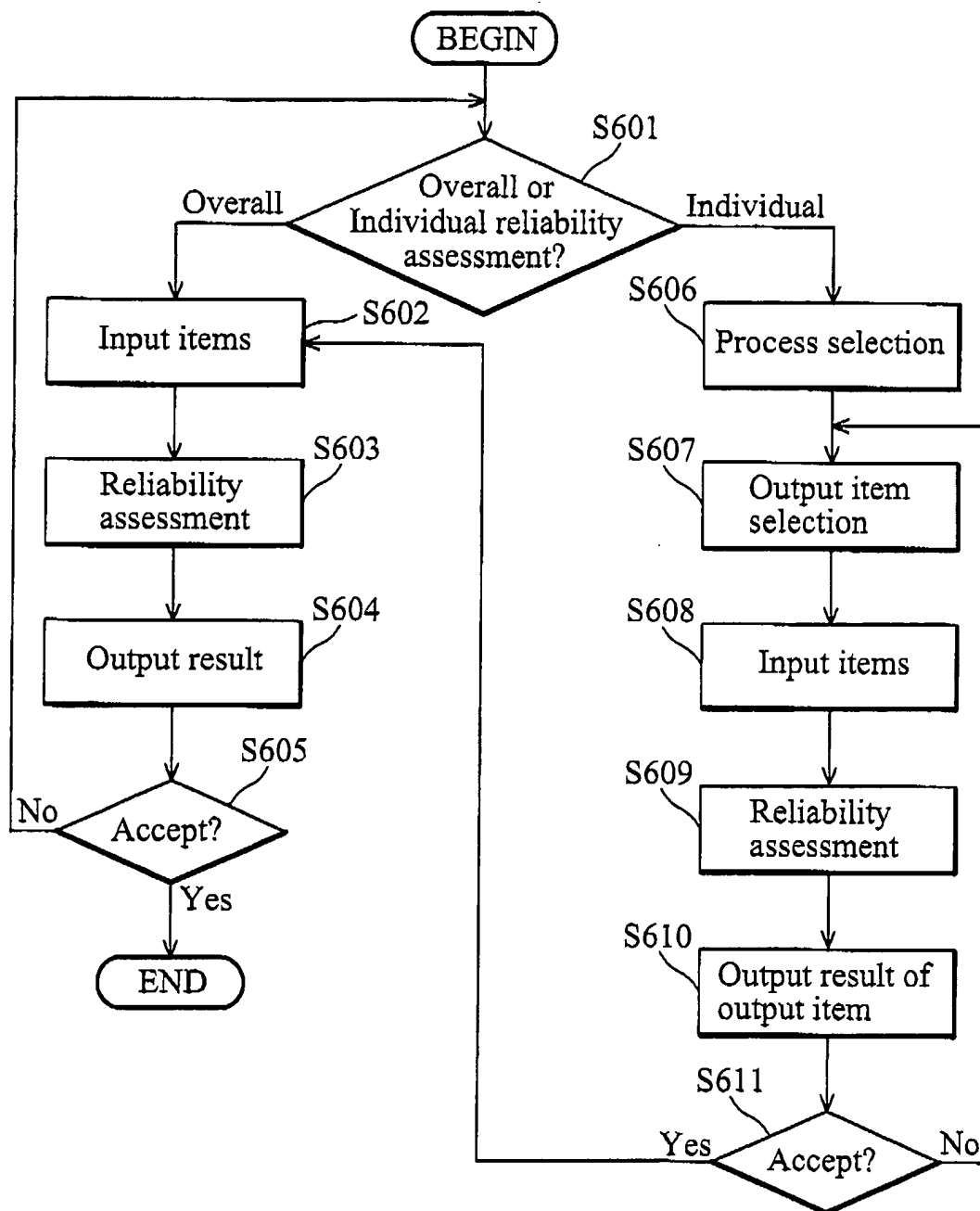


FIG. 6

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Items	Input
	[v] 0.13um, [] 90nm
*Generation	[] CL013G (1.2V/3.3V) FSG, [] CL013LV (1.0V/3.3V) FSG, [] CL013G (1.2V/3.3V) LK, [v] CL013LV (1.0V/3.3V) LK
*Process	[1] Poly [8] Metal
*Vcc	core [1.0] V, I/O [3.3] V
*Tj max	[85] C tolerance [nm] C
*Gate oxide area (in total product)	core NMOS [2E6] μm^2 , core PMOS [2E6] μm^2 I/O NMOS [2E6] μm^2 , I/O PMOS [2E6] μm^2
Transistor size	core NMOS: W/L=[10]/[0.13] μm core PMOS: W/L=[10]/[0.13] μm I/O NMOS: W/L=[10]/[0.35] μm I/O PMOS: W/L=[10]/[0.3] μm
Metal dimension	metal-1 : spacing/length = [0.18]/[0.00] μm inter-metal (M2~M7): spacing/length = [0.21]/[0.00] μm top metal (M8): spacing/length = [0.46]/[0.00] μm
*Use TSMC EM Jmax design rule	[100%]
Product lifetime	[10] years
Product burn-in	[NO], If "YES", then Vcc = [] V with duration [] hrs
Product die size	X = [xxx] mm, Y = [yyy] mm (no including scribe line and seal ring)
Emb-SRAM size/area	[aaa] Mbits with area [bbb] mm^2
EFR expection	[500] DPM with duration [30] days
Excute	

700

FIG. 7

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Customer: MEI		User: Tony_Lee	Sheet no. 00001	
Process	Items	Device	Dimension	Decision
Reliability	GOI	core NMOS	2E6 μm^2	pass
		core PMOS	2E6 μm^2	pass
		I/O NMOS	2E6 μm^2	pass
		I/O PMOS	2E6 μm^2	pass
		core NMOS	10/0.13	pass
	HCI	core PMOS	10/0.13	pass
		I/O NMOS	10/0.35	fail
		I/O PMOS	10/0.3	pass
		core PMOS	10/0.13	pass
		I/O PMOS	10/0.3	pass
Process	EM	metal line		pass
		contact/via hole		pass
		bump		pass
		IMD		pass
		LK IMD TDDB		pass
	EFR	30 days		---
		0-1 year		---
		1-10 years		---
Reliability	NBTI	core PMOS	10/0.13	pass
		I/O PMOS	10/0.3	pass
		core PMOS	10/0.13	pass
		I/O PMOS	10/0.35	fail
		I/O PMOS	10/0.3	pass
	EM	metal line		pass
		contact/via hole		pass
		bump		pass
		IMD		pass
		LK IMD TDDB		pass
Process	EFR	30 days		---
		0-1 year		---
		1-10 years		---
	LTFA	500 DPM		---
		200 FITs		---
		800 FITs		---

800

810

Fig. 8A Fig. 8B

FIG. 8A

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Date: July 1, 2003
Criterion
0.1% cum. fail, DC >= 10 years
delta Idsh >= 2.5%, 0.1% cum. fail, DC >= 0.2 years
delta Idsat >= 10%, 0.1% cum. fail, DC >= 0.2 years
delta Idsat >= 10%, 0.1% cum. fail, DC >= 5 years
delta R <= 10%, DC > 10 years
0.1% cum. fail, DC >= 10 years

FIG. 8B

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Items	Input	output
Generation	[v] 0.13um, [] 90nm	0.13um
Process	[v] 1.2V/3.3V FSG, [] 1.0V/3.3V FSG, [] 1.2V/3.3V LK, [] 1.0V/3.3V LK	1.2V/3.3V FSG
Choose output item	[] DC lifetime [] transistor size [] cum. fail [] Tj max [v] Vcc	Vcc
Vcc	core [] V, I/O [] V tolerance [0.1] V	core <= 1.2 V, I/O <= 3.5 V
Tj max	[85] C tolerance [nm] C	85 C
Transistor size	core NMOS : W/L=[10] / [0.13] um core PMOS : W/L=[10] / [0.13] um I/O NMOS : W/L=[10] / [0.35] um I/O PMOS : W/L=[10] / [0.30] um	core NMOS : W/L=10/0.13 um core PMOS : W/L=10/0.13 um I/O NMOS : W/L=10/0.35 um I/O PMOS : W/L=10/0.30 um
Fail criterion	[v] Idsat with [10] % degradation (Vs=Vb=GND, Vd=Vg=Vcc) [] Idlin with [] % degradation (Vs=Vb=GND, Vd=0.1V, Vg=Vcc) [] gm with [] % degradation (Vs=Vb=GND, Vd=0.1V, sweep Vg) [] Vt with [] % degradation (Vs=Vb=GND, Vd=0.1V, sweep Vg)	delta Idsat >= 10%
cum fail (%)	[0.1] %	0.1%
DC lifetime	[0.2] years	0.2 years
DC to AC factor	[50] or [] (please provide wave form excel file)	DC to AC factor = 50
Excute		

900

910

FIG. 9

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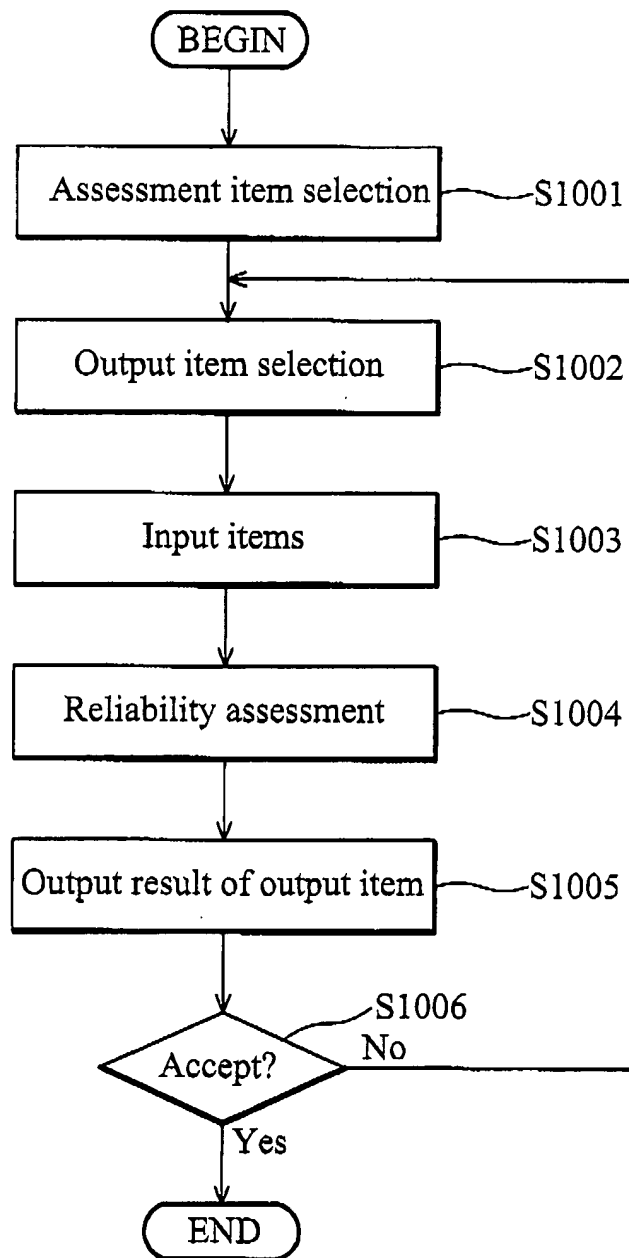


FIG. 10

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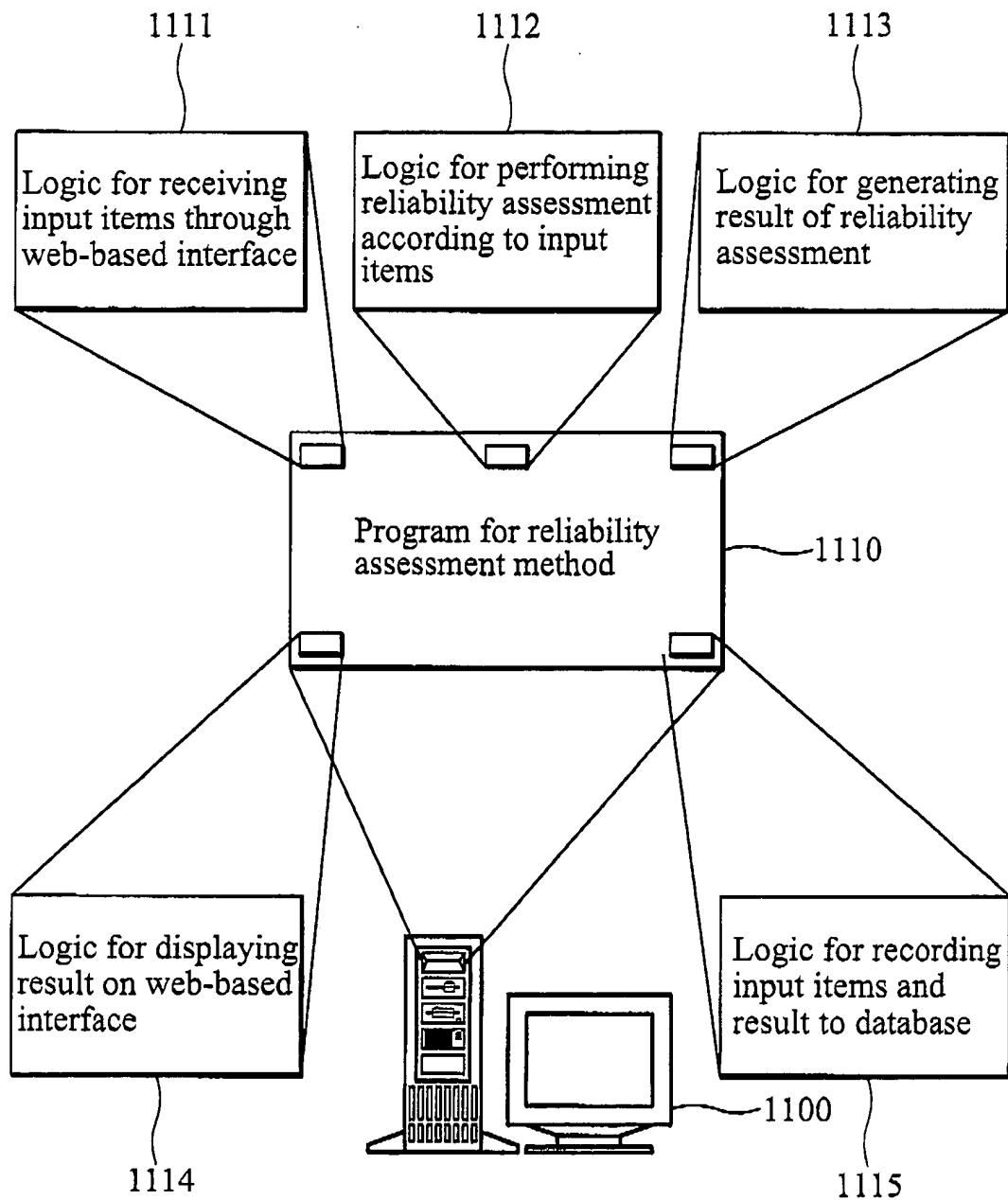


FIG. 11